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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,462	03/15/2004	Dimitri C. Argyres	002489.P042	3222

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EXAMINER	
MOORE, PATRICK M	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 09/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,462	ARGYRES ET AL.	
	Examiner	Art Unit	
	Patrick M. Moore	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,2,14-17,24-26 and 33* is/are rejected.

7)☐ Claim(s) *3-13,18-23,27-32,34 and 35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/22/04&3/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-35 have been examined.

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on 22 July 2004 and 15 May 2004 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Drawings

3. The drawings were received on 02 July 2004. These drawings are acceptable.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 14-17, 24-26 & 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Abbott (US Patent # 6,121,791).

a. **As per Claim 1**, Abbott discloses an apparatus, comprising: control logic comprising a plurality of logic cells, at least one of the plurality of logic cells configured to receive an A operand and a B operand **[input array as per Column 5, Lines 23-28 & Figure 1, #108]** and perform the following logic operations comprising [overscore (A)]B, A[overscore (B)], and AB **[selective negation using logic elements as per Column 8, Lines 4-13 & Figure 2, #210]**; and switch circuitry coupled to receive input data, the switch circuitry

coupled to the control logic to receive a result of the AB logic operation from each of the plurality of logic cells and selectively enable the output of one or more bits of the input data based on the result of the AB logic operation **[Figure 2, #202 & Column 7, Lines 30-35]**.

b. **As per Claim 2**, Abbott discloses an apparatus of claim 1, wherein the control logic is coupled to receive a first plurality of enable signals, each of the first plurality of first enable signals corresponding to a first plurality of one or more bits of a first segment of the input data **[control bit as per Column 7, Lines 35-51]**, and wherein the control logic is coupled to receive a second plurality of enable signals, each of the second plurality of enable signals corresponding to a second plurality of one or more bits of a second segment of the input data **[different control bit as per Column 7, Lines 52-60]**.

c. **As per Claim 14**, Abbott further discloses the apparatus of claim 1, wherein at least another of the plurality of logic cells is configured to receive a result of the [overscore (A)]B logic operation of the at least one logic cell and an enable signal as the B operand, and wherein the at least another of the plurality of logic cells is configured to perform the AB logic operation **[Programmable Logic Datapath as per Column 3, Lines 9-19, Figure 1, #114 & column 4, Lines 4-13]**.

d. **As per Claim 15**, Abbott discloses a method, comprising: providing a matrix of M rows and N columns of logic cells in a content addressable memory (CAM) device, where N is equal to or greater than 1 and M is greater than 1 **[32 bits**

wide and 256 bits deep as per Column 4, Line 60 – Column 5, Line 6 & Figure 1, #104 & 106]; and performing an AB logic operation in each of the logic cells **[Programmable Logic Datapath as per Column 3, Lines 9-19, Figure 1, #114 & column 4, Lines 4-13]**.

e. **As per Claim 16**, Abbott further discloses the method of claim 15, further comprising: selecting among a second one or more bits of input data using a result of the AB logic operation in at least one of the logic cells **[selector unit as per Figure 1, #108 & Column 5, Lines 12-22]**; and selecting between the selected second one or more bits of input data and a first one or more bits of input data for output to a comparand in the CAM device **[output array as per Figure 1, #118 & Column 5, Lines 15-22]**.

f. **Claim 17** is rejected under identical grounds as Claim 2.

g. **As per Claim 24**, Abbott discloses a content addressable memory (CAM) device, comprising: a matrix of M rows and N columns of logic cells, where N is equal to or greater than 1 and M is greater than 1 **[32 bits wide and 256 bits deep as per Column 4, Line 60 – Column 5, Line 6 & Figure 1, #104 & 106]**; and means for performing an AB logic operation in each of the logic cells **[Programmable Logic Datapath as per Column 3, Lines 9-19, Figure 1, #114 & column 4, Lines 4-13]**.

h. **As per Claim 25**, Abbott further discloses the CAM device of claim 24, further comprising: means for selecting among a second one or more bits of input data

using a result of the AB logic operation in at least one of the logic cells **[selector unit as per Figure 1, #108 & Column 5, Lines 12-22]**; and means for selecting between the selected second one or more bits of input data and a first one or more bits of input data for output to a comparand in the CAM device **[output array as per Figure 1, #118 & Column 5, Lines 15-22]**.

i. **As per Claim 26**, Abbott discloses a content addressable memory (CAM) device, comprising: a CAM array coupled to receive a comparand **[Column 4, Line 60 – Column 5, Line 6 & Figure 1, #104 & 106]**; and a filter circuit coupled to the CAM array, wherein the filter circuit is coupled to receive input data **[selector unit as per Figure 1, #108 & Column 5, Lines 12-22]**, the input data including a first one or more bits having a first order position and a second one or more bits having a second order position being one of lower than or higher than the first order position **[input array as per Column 5, Lines 23-28 & Figure 1, #108]**, wherein the filter circuit is configured to provide the first one or more bits to the comparand in the first order position and transpose the second one or bits of the input data to a third order position in the comparand, the third order position being the other of the lower than or higher than the first order position **[depth of subfield addresses as applied to control the logical datapath as per Column 5, Lines 39-61]**.

j. **As per Claim 33**, Abbott discloses a method in a content addressable memory (CAM) device, comprising: receiving input data including a first one or more bits having a first order position and a second one or more bits having a second order

position being one of lower than or higher than the first order position **[input array as per Column 5, Lines 23-28 & Figure 1, #108]**; providing the first one or more bits to a comparand in the first order position **[sub-fields as per Column 5, Lines 28-38]**; and transposing the second one or bits of the input data to a third order position in the comparand, the third order position being the other of the lower than or higher than the first order position **[depth of subfield addresses as applied to control the logical datapath as per Column 5, Lines 39-61]**.

Allowable Subject Matter

5. Claims 3-13, 18-23, 27-32 & 34-35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick M. Moore whose telephone number is (571) 272-1239. The examiner can normally be reached on M-F 8:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabahn can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PMM

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER
9/5/07